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To: U.S. Department of Commerce
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Atty. Dkt. No.	M#	Client Ref.
	307277	7048P-U1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Applicant: INAGAKI, Yasushi et al.

Divisional of Appln. No.: 09/830,360 filed 4/25/01

Filing Date: February 18, 2004

Date: February 19, 2004 Page 1 of 1

Examiner: TBA Group Art Unit: TBA

U.S. PATENT DOCUMENTS

Examiner's Initials*		Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
	AR	5,027,253	06/1991	Lauffer et al.			
	BR	5,559,363	09/1996	Immorlica, Jr., Anthony A.			
	CR	5,565,706	10/1996	Miura et al.			
	DR	5,745,984	05/1998	Cole et al.			
	ER	5,875,100	02/1999	Yamashita, Koji			
	FR	6,021,050	02/2000	Ehman et al.			
	GR	6,153,290	11/2000	Sunahara, Hirofumi			
	HR						
	IR						

FOREIGN PATENT DOCUMENTS

		Document Number	Date MM/YYYY	Country	Inventor Name		English Abstract		Translation Readily Available	
							Enclosed	No	Enclose	No
	JR	11-248311	09/1999	Japan	Sakano et al.					
	KR	6-326472	11/1994	Japan	Furusawa					
	LR	7-263619	10/1995	Japan	Ito					
	MR	10-256429	09/1998	Japan	Iyogi et al.					
	NR	11-45955	06/1989	Japan	Makiura					
	OR	11-126978	05/1999	Japan	Fujisaki					
	PR	11-312868	11/1999	Japan	Hayashi					
	QR									
	RR									
	SR									

OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

	TR	PATENT ABSTRACTS OF JAPAN, "MULTILAYERED WIRING BOARD" JP 11-126978, May 11, 1999, Akiya.Fujisaki et al
	UR	PATENT ABSTRACTS OF JAPAN " METHOD FOR MANUFACTURING MULTILAYER PRINTED WIRING BOARD ", JP 10-013024, January 1, 1998, Satoshi Nakamura
	VR	PATENT ABSTRACTS OF JAPAN, "ELECTRODE STRUCTURE AND THE MANUFACTURING METHOD", JP 54-157296, December 12, 1979
	WR	PATENT ABSTRACTS OF JAPAN, " MULTILAYER ELECTRONIC PART AND MANUFACTURE THEREOF ", JP 8-241827, September 17, 1996
	XR	

Examiner Date Considered:

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

Inventor(s): INAGAKI et al.
Atty.Dkt: 041226/0307277 Group Art Unit: TBA
Appln. No.: NEW APPLICATION Examiner: TBA
Filed: February 19, 2004
FOR: PRINTED CIRCUIT BOARD AND METHOD OF MANUFACTURING PRINTED CIRCUIT BOARD

Date: February 19, 2004

IDS LETTER CITING APPLICATION(S)

The Examiner's attention is directed to the following application(s) of:

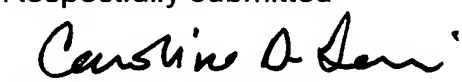
Examiner's Initials*	FIRST INVENTOR (Last Name Only)	APPLICATION NO. & Filing Date	ENCLOSED
	INAGAKI	09/830,361 April 25, 2001	☐ Spec ☐ Drawings ☐ Current Claims ☐ Other

PLEASE DO NOT PRINT the above information on the patent which results from the subject application.

Consideration of the above listed application is earnestly solicited since unpublished patent applications are contemplated as IDS material; see the exception in Rule 98(a)(2)(iii) and note the penultimate sentence of MPEP 609.

Further, in keeping with MPEP 609, Subsec. C(2), 2nd para., line 10 to end of the paragraph (especially note lines 18-25) **PLEASE RETURN A COPY OF THIS LETTER** with the Examiner's initials adjacent each above listing so that applicant will know that the application listed above has been considered as required by PTO policy.

Respectfully submitted



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*The Examiner's initials adjacent a citation indicates he/she has considered the cited application relative to the subject application.